AiP74LVT/LVTH245
Octal Bus Transceiver; 3-state

Product Specification

Specification Revision History：

Version	Date	Description
2017-12-A1	2017-12	New
2023-04-B1	2023-04	Update the template
2025-02-B2	2025-02	Modify the content

Contents

1、General Description

The AiP74LVT245; AiP74LVTH245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. It features an output enable ($\overline{OE}$) input for easy cascading and a direction (DIR) input for direction control.

Features:

- 3-state buffers
- Octal bidirectional bus interface
- Input and output interface capability to systems at 5V supply
- Output capability: +64mA/-32mA
- Bus-hold data inputs eliminate the need for external pull-up resistors for unused inputs
- Live insertion/extraction permitted
- I_{OFF} and Power-up 3-state support Hot insertion
- No bus current loading when output is tied to 5V bus
- Specified from -40℃ to +125℃
- Packaging information:SOP20/TSSOP20/DHVQFN20

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVT245SA20.TB	SOP20	74LVT245	35 PCS/tube	80 tube/box	2800 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm
AiP74LVTH245SA20.TB	SOP20	74LVTH245	35 PCS/tube	80 tube/box	2800 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm
AiP74LVT245TA20.TB	TSSOP20	74LVT245	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm
AiP74LVTH245TA20.TB	TSSOP20	74LVTH245	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVT245SA20.TR	SOP20	74LVT245	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing:1.27mm
AiP74LVTH245SA20.TR	SOP20	74LVTH245	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing:1.27mm
AiP74LVT245TA20.TR	TSSOP20	74LVT245	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing:0.65mm
AiP74LVTH245TA20.TR	TSSOP20	74LVTH245	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing:0.65mm
AiP74LVT245QE20.TR	DHVQFN20	74LVT245	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 4.5mm×2.5mm Pin spacing:0.5mm
AiP74LVTH245QE20.TR	DHVQFN20	74LVTH245	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 4.5mm×2.5mm Pin spacing:0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

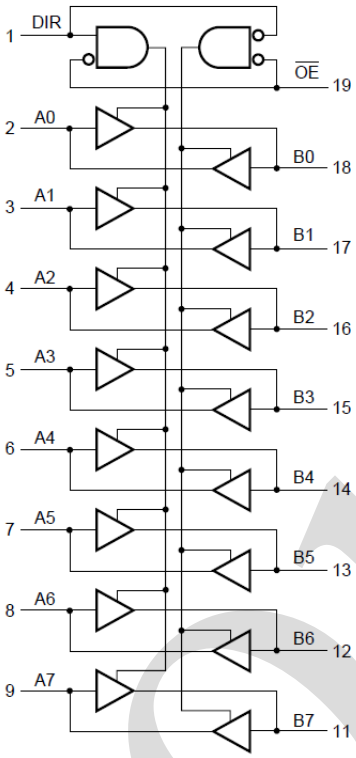


Figure 1. Logic symbol

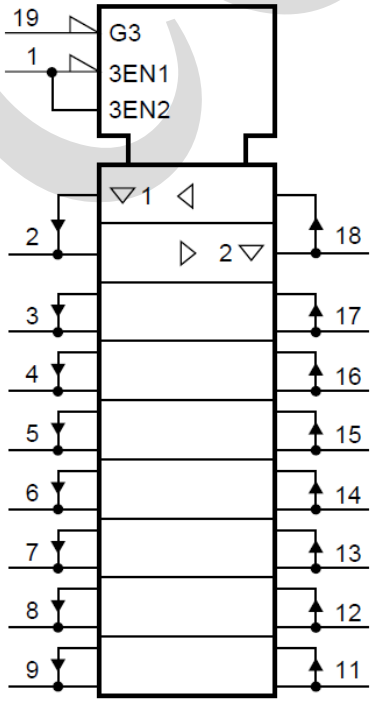
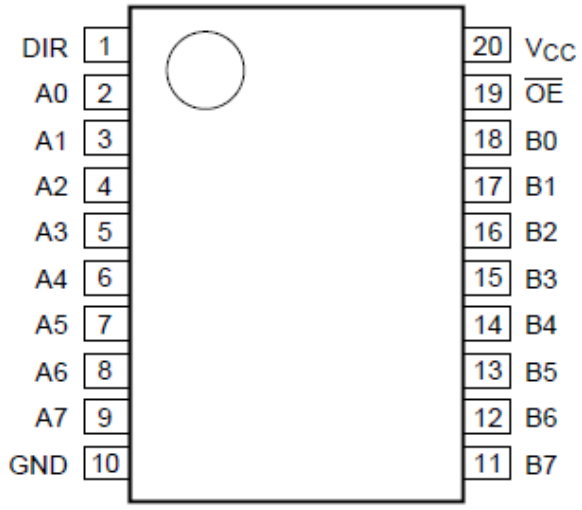
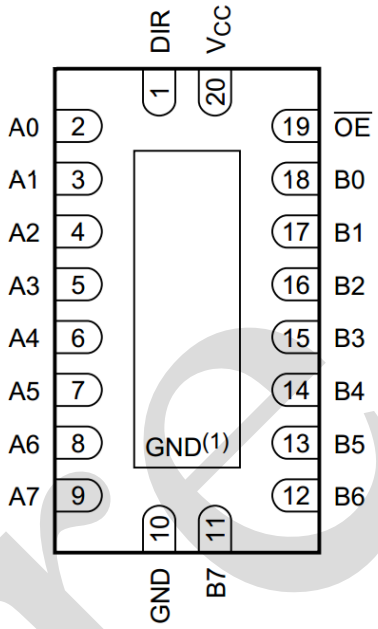


Figure 2. IEC logic symbol

2.2、Pin Configurations



SOP20 and TSSOP20



DHVQFN20

Note:
(1) The die substrate is attached to this pad using a conductive die attach material. It can not be used as a supply pin or input.

2.3、Pin Description

Pin No.	Pin Name	Description
1	DIR	direction control
2,3,4,5,6,7,8,9	A0 to A7	data inputs/outputs
10	GND	ground (0V)
18,17,16,15,14,13,12,11	B0 to B7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	supply voltage

2.4、Function Table

Inputs		Inputs/outputs	
$\overline{OE}$	DIR	An	Bn
L	L	An=Bn	Inputs
L	H	Inputs	Bn=An
H	X	Z	Z

Note:
H=HIGH voltage level;
L=LOW voltage level;
X=don't care;
Z=high impedance OFF-state.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.) [1][2]

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7.0	V
input voltage	V_I	-[3]	-0.5	+7.0	V
output voltage	V_O	output in OFF or HIGH state[3]	-0.5	+7.0	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
output clamping current	I_{OK}	V_O<0V	-50	-	mA
output current	I_O	output in LOW state	-	128	mA
		output in HIGH state	-64	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
junction temperature	T_j	-	-	+150	℃
total power dissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	260		℃

Note:

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150℃.

[3] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.7	-	5.5	V
input voltage	V_I	-	0	-	5.5	V
HIGH-level output current	I_{OH}	-	-	-	-32	mA
LOW-level output current	I_{OL}	-	-	-	32	mA
		current duty cycle≤50%; f_i≥1kHz	-	-	64	mA
ambient temperature	T_{amb}	in free air	-40	-	+125	℃
input transition rise and fall rate	Δt/ΔV	output enabled	-	-	10	ns/V

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
input clamping voltage	V_{IK}	V_{CC}=2.7V; I_{IK}= -18mA		-1.2	-0.9	-	V
HIGH-level input voltage	V_{IH}	-		2.0	-	-	V
LOW-level input voltage	V_{IL}	-		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_{CC}=2.7V to 3.6V; I_{OH}= -100uA		V_{CC}-0.2	V_{CC}-0.1	-	V
		V_{CC}=2.7V; I_{OH} = -8mA		2.4	2.5	-	V
		V_{CC}=3.0V; I_{OH} = -32mA		2.0	2.2	-	V
LOW-level output voltage	V_{OL}	V_{CC}=2.7V; I_{OL}=100uA		-	0.1	0.2	V
		V_{CC}=2.7V; I_{OL}=24mA		-	0.3	0.5	V
		V_{CC}=3.0V; I_{OL}=16mA		-	0.25	0.4	V
		V_{CC}=3.0V; I_{OL}=32mA		-	0.3	0.5	V
		V_{CC}=3.0V; I_{OL}=64mA		-	0.4	0.55	V
input leakage current	I_I	control pins	V_{CC}=0V or 3.6V; V_I=5.5V	-	-	10	uA
			V_{CC}=3.6V; V_I=V_{CC} or GND	-	-	±1	uA
		I/O data pins[2]	V_{CC}=3.6V; V_I=5.5V	-	-	20	uA
			V_{CC}=3.6V; V_I=V_{CC}	-	-	1	uA
			V_{CC}=3.6V; V_I=0V	-5	-	-	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=0V to 4.5V		-	-	±100	uA
output leakage current	I_{LO}	V_O=5.5V; V_{CC}=3.6V; output HIGH		-	-	125	uA
power-up/ power-down output current	$I_{O(pu/pd)}$	V_{CC}≤1.2V; V_O=0.5V to V_{CC}; V_I=GND or V_{CC}; $\overline{OE}$ =don't care[3]		-	-	±100	uA
bus hold LOW current	I_{BHL}	V_{CC}=3.0V; V_I=0.8V		75	150	-	uA
bus hold HIGH current	I_{BHH}	V_{CC}=3.0V; V_I=2.0V		-	-150	-75	uA
bus hold LOW overdrive current	I_{BHLO}	V_{CC}=0V to 3.0V; V_I=3.6V[4]		500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	V_{CC}=0V to 3.0V; V_I=3.6V[4]		-	-	-500	uA
supply current	I_{CC}	V_{CC}=3.6V; V_I=V_{CC} or GND; I_O=0A	outputs HIGH	-	-	0.19	mA
			outputs LOW	-	-	0.19	mA
			outputs disabled	-	-	0.19	mA
additional supply current	ΔI_{CC}	per input pin; V_{CC}=3.0V to 3.6V; one input = V_{CC}-0.6V; other inputs at V_{CC} or GND[5]		-	-	0.2	mA

Input capacitance	C_I	DIR and $\overline{OE}$ inputs;outputs disabled;V_I=0Vor 3.0V	-	4	-	pF
input/output capacitance	$C_{I/O}$	at input/output data pins,outputs disabled;$V_{I/O}$ = 0Vor 3.0V	-	10	-	pF

Note:

[1] All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25℃.

[2] Unused pins at V_{CC} or GND.

[3] This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10ms. From V_{CC}=1.2V to V_{CC}=3.3V±0.3V a transition time of 100ms is permitted. This parameter is valid for T_{amb}=+25℃ only.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
input clamping voltage	V_{IK}	V_{CC}=2.7V; I_{IK}= -18mA		-1.2	-	-	V
HIGH-level input voltage	V_{IH}	-		2.0	-	-	V
LOW-level input voltage	V_{IL}	-		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_{CC}=2.7V to 3.6V; I_{OH}= -100uA		V_{CC}-0.2	-	-	V
		V_{CC}=2.7V; I_{OH} = -8mA		2.4	-	-	V
		V_{CC}=3.0V; I_{OH} = -32mA		2.0	-	-	V
LOW-level output voltage	V_{OL}	V_{CC}=2.7V; I_{OL}=100uA		-	-	0.2	V
		V_{CC}=2.7V; I_{OL}=24mA		-	-	0.5	V
		V_{CC}=3.0V; I_{OL}=16mA		-	-	0.4	V
		V_{CC}=3.0V; I_{OL}=32mA		-	-	0.5	V
		V_{CC}=3.0V; I_{OL}=64mA		-	-	0.55	V
input leakage current	I_I	control pins	V_{CC}=0V or 3.6V; V_I=5.5V	-	-	10	uA
			V_{CC}=3.6V; V_I=V_{CC} or GND	-	-	±1	uA
		I/O data pins[2]	V_{CC}=3.6V; V_I=5.5V	-	-	20	uA
			V_{CC}=3.6V; V_I=V_{CC}	-	-	1	uA
			V_{CC}=3.6V; V_I=0V	-5	-	-	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=0V to 4.5V		-	-	±100	uA
output leakage current	I_{LO}	V_O=5.5V; V_{CC}=3.6V; output HIGH		-	-	125	uA
power-up/ power-down output current	$I_{O(pu/pd)}$	V_{CC}≤1.2V; V_O=0.5V to V_{CC}; V_I=GND or V_{CC}; $\overline{OE}$ =don't care[3]		-	-	±100	uA

bus hold LOW current	I_{BHL}	V_{CC}=3.0V; V_I=0.8V		75	-	-	uA
bus hold HIGH current	I_{BHH}	V_{CC}=3.0V; V_I=2.0V		-	-	-75	uA
bus hold LOW overdrive current	I_{BHLO}	V_{CC}=0V to 3.0V; V_I=3.6V[4]		500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	V_{CC}=0V to 3.0V; V_I=3.6V[4]		-	-	-500	uA
supply current	I_{CC}	V_{CC}=3.6V; V_I=V_{CC} or GND; I_O=0A	outputs HIGH	-	-	0.19	mA
			outputs LOW	-	-	0.19	mA
			outputs disabled	-	-	0.19	mA
additional supply current	ΔI_{CC}	per input pin; V_{CC}=3.0V to 3.6V; one input = V_{CC}-0.6V; other inputs at V_{CC} or GND[5]		-	-	0.2	mA

Note:

[1] All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25℃.

[2] Unused pins at V_{CC} or GND.

[3] This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10ms. From V_{CC}=1.2V to V_{CC}=3.3V±0.3V a transition time of 100ms is permitted. This parameter is valid for T_{amb}=+25℃ only.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
LOW to HIGH propagation delay	t_{PLH}	An to Bn or Bn to An	V_{CC}=2.7V	-	-	6.6	ns
			V_{CC}=3.3V±0.3V	1.0	3.4	5.6	ns
HIGH to LOW propagation delay	t_{PHL}	An to Bn or Bn to An	V_{CC}=2.7V	-	-	6.4	ns
			V_{CC}=3.3V±0.3V	1.0	3.4	5.6	ns
OFF-state to HIGH propagation delay	t_{PZH}	see Figure 5	V_{CC}=2.7V	-	-	9.9	ns
			V_{CC}=3.3V±0.3V	1.1	4.6	7.7	ns
OFF-state to LOW propagation delay	t_{PZL}	see Figure 5	V_{CC}=2.7V	-	-	9.1	ns
			V_{CC}=3.3V±0.3V	1.1	4.6	7.7	ns
HIGH to OFF-state propagation delay	t_{PHZ}	see Figure 5	V_{CC}=2.7V	-	-	9.1	ns
			V_{CC}=3.3V±0.3V	2.2	5.0	8.3	ns
LOW to OFF-state propagation delay	t_{PLZ}	see Figure 5	V_{CC}=2.7V	-	-	6.7	ns
			V_{CC}=3.3V±0.3V	2.0	4.8	6.7	ns

Note:

[1] Typical values are measured at T_{amb}=25℃ and V_{CC}=3.3V.

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
LOW to HIGH propagation delay	t_{PLH}	An to Bn or Bn to An	V_{CC}=2.7V	-	-	7.8	ns
			V_{CC}=3.3V±0.3V	-	-	6.7	ns
HIGH to LOW propagation delay	t_{PHL}	An to Bn or Bn to An	V_{CC}=2.7V	-	-	7.7	ns
			V_{CC}=3.3V±0.3V	-	-	6.7	ns
OFF-state to HIGH propagation delay	t_{PZH}	see Figure 5	V_{CC}=2.7V	-	-	11.9	ns
			V_{CC}=3.3V±0.3V	-	-	9.2	ns
OFF-state to LOW propagation delay	t_{PZL}	see Figure 5	V_{CC}=2.7V	-	-	10.9	ns
			V_{CC}=3.3V±0.3V	-	-	9.2	ns
HIGH to OFF-state propagation delay	t_{PHZ}	see Figure 5	V_{CC}=2.7V	-	-	10.9	ns
			V_{CC}=3.3V±0.3V	-	-	9.9	ns
LOW to OFF-state propagation delay	t_{PLZ}	see Figure 5	V_{CC}=2.7V	-	-	8.1	ns
			V_{CC}=3.3V±0.3V	-	-	8.1	ns

Note:

[1] Typical values are measured at T_{amb}=25℃ and V_{CC}=3.3V.

4、Testing Circuit

4.1、AC Testing Circuit

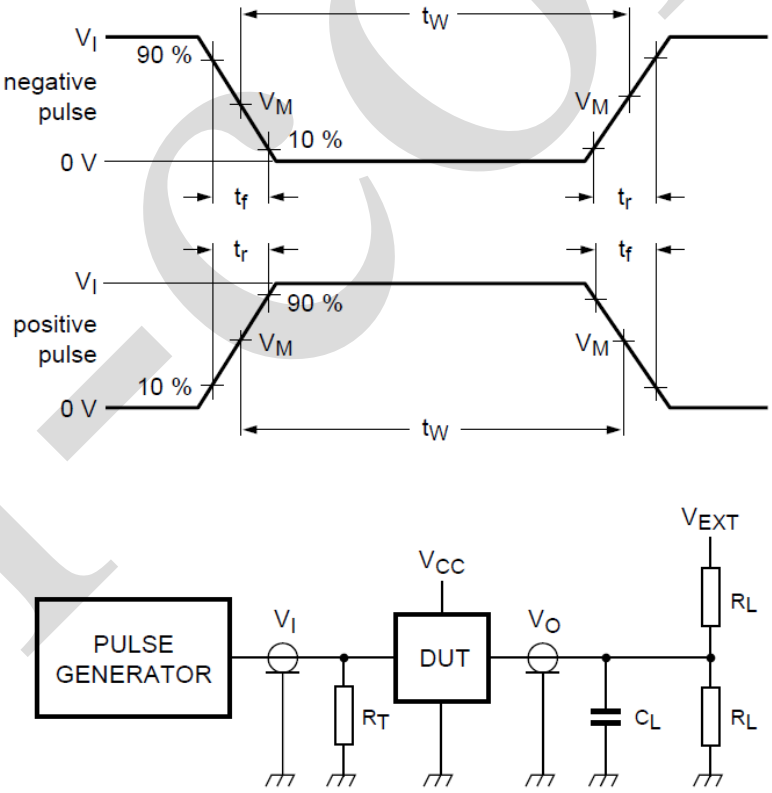


Figure 3. Test circuit for switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

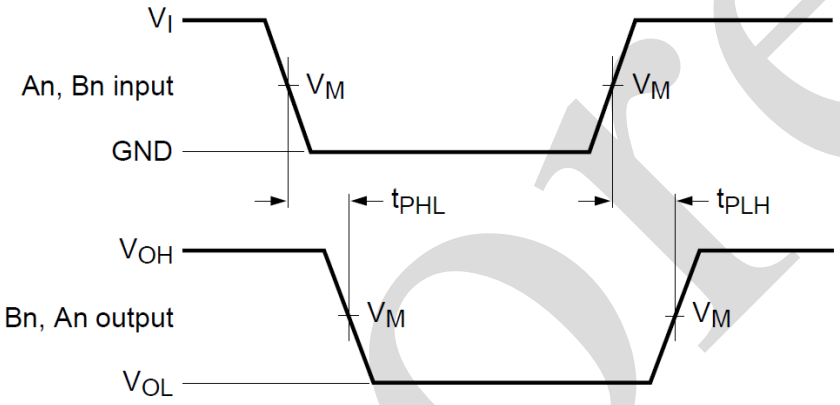
R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT}=External voltage for measuring switching times.

4.2、Test Data

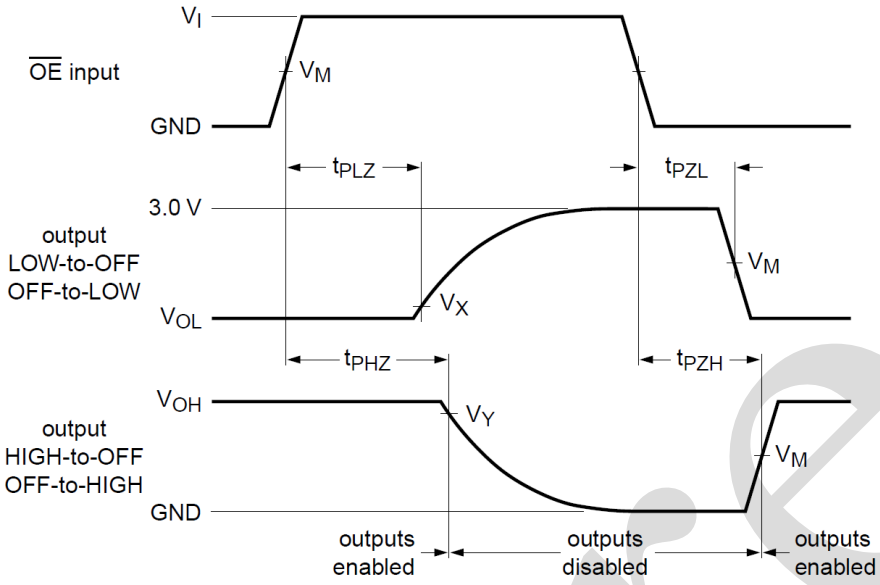
Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r , t_f	R_L	C_L	t_{PHZ} , t_{PZH}	t_{PLZ} , t_{PZL}	t_{PLH} , t_{PHL}
2.7V	≤10MHz	500ns	≤2.5ns	500Ω	50pF	GND	6V	open

4.3、AC Testing Waveforms



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Input (An, Bn) to output (Bn, An) propagation delays and output transition times



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

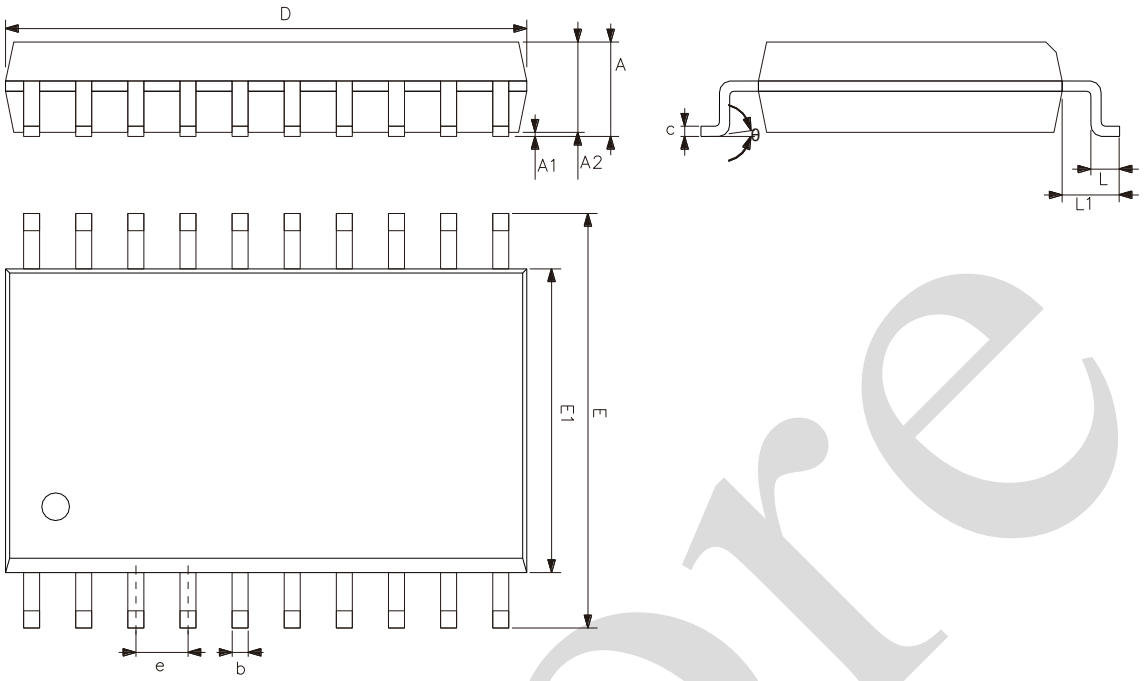
Figure 5. 3-state output enable and disable times

4.4、Measurement Points

V_{CC}	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
2.7V to 3.6V	GND to 2.7V	1.5V	1.5V	V_{OL}+0.3V	V_{OH}-0.3V

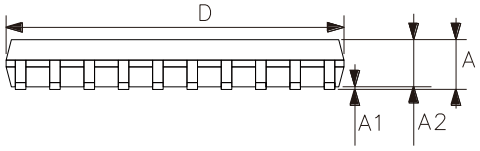
5、Package Information

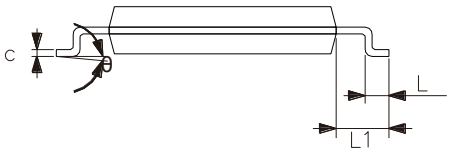
5.1、SOP20

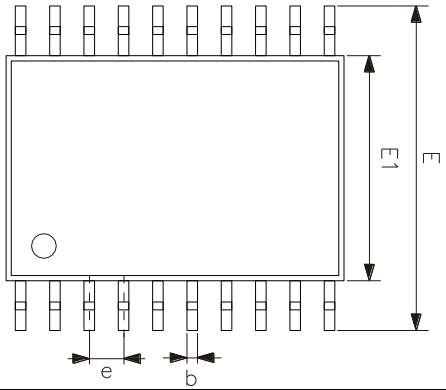


Symbol	Dimensions (mm)	
	Min.	Max.
A	2.47	2.65
A1	0.05	0.30
A2	2.20	2.44
b	0.35	0.50
c	0.15	0.30
D	12.54	12.94
E	10.00	10.60
E1	7.30	7.70
e	1.27	
L	0.40	1.05
L1	1.30	1.50
θ	0 °	8 °

5.2、TSSOP20

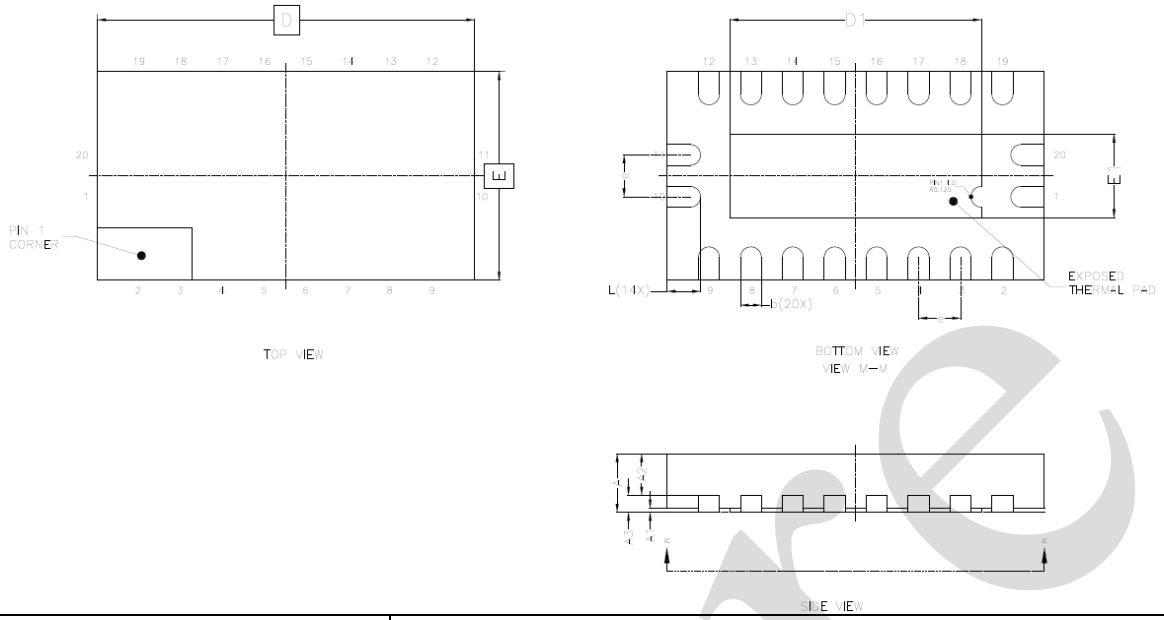






Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

5.3、DHVQFN20



Symbol	Dimensions (mm)	
	Min.	Max.
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.70
A3	0.20	
D	4.40	4.60
E	2.40	2.60
e	0.50	
b	0.18	0.30
L	0.30	0.50
D1	2.70	3.15
E1	0.70	1.15

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We Recommend you to read this chapter carefully before using this product.

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